Computer Science and Engineering

Semester/Year		Program		B.Tech.
Subject Category	ESC	Subject Code: CSA102	Subject Name:	Digital Electronics

Maximum Marks Allotted								Contact Hours			Total Credits
Theory				Practical			Total Marks				
End Sem	Mid-Sem	Assign ment	Quiz	End Sem	Lab-Work	Quiz		L	T	P	
60	20	10	10	--	--	--	100	3	0	0	3

Prerequisites:

Basics of Physics

Course Objective:

The objective of this course is to provide the fundamental concepts associated with the digital logic and circuit design. To familiarize students with the different number systems, logic gates, minimization of logic circuits and combinational and sequential circuits utilized in the different digital circuits and systems. The course will help student to design and analyze the digital circuits and systems.

Course Outcomes:

Upon completion of this course, the student will be able to:

- CO1: Convert different number systems and codes used in digital circuits and systems.
- CO2: Simplify and analyze the digital logic circuits using Boolean algebra and other mapping techniques.
- CO3: Analyse and design different combinational logic circuits using different mapping techniques and mathematical tools.
- CO4: Compare different types of sequential circuits viz. counters in the domain of analysis.

UNITs	Descriptions	Hrs.	CO's
I	**Introduction to Digital Electronics**: Review of number system and conversions; Binary Arithmetic, Signed and Unsigned representation, Binary codes, Gray Code, Code Conversions, Error detection and correction codes - parity check codes and Hamming code.	8	CO1
II	**Boolean Algebra and Switching Functions** - Study of basic logic gates, Basic postulates and fundamental theorems of Boolean algebra; Standard representation of logic functions - SOP and POS forms; Simplification of switching functions - K-map and Quine-McCluskey tabular methods.	8	CO2
III	**Combinational Logic Modules and their applications**: Adders, Subtractors, Code Converters, parity generators and comparators, Encoders & Decoders, BCD to seven-segment decoder, Multiplexers & Demultiplexers and their applications.	9	CO3
IV	**Sequential Circuits and Systems:** Set-Reset latches and flip flops, D-flipflop, R-S flip-flop, J-K Flip-flop, Master slave Flip flop, edge triggered flip-flop, T flip-flops, Shift registers, classification of shift registers.	7	CO4
V	**Counters classification**: asynchronous counters, synchronous counters, counters design, BCD counter, MOD counters, ripple counter, Introduction to finite state machines.	8	CO4
Guest Lectures (if any)		--	
Total Hours		40	

Dr. Kanak Saxena
Chairperson

List of Experiments

S.A.T.I.

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VIDISHA M.P.
योगः कर्मसु कौशलम्

Name	PIYUSH AGRAWAL
Class	B. TECH (I.T.)
Subject	DIGITAL ELECTRONIC
Year	2022 - 2023
Sch. No.	33006

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Expt No.	EXPERIMENT JOB	Date of Performance	Date of Submission	Remarks	Grade	Sig. of Student	Signature Teacher
1.	Number System	14/11/22	21/11/22			Piyush	
2.	LOGIC GATES	27/11/22	04/12/22			Piyush	
3.	COMBINATIONAL CIRCUIT	09/12/22	18/12/22			Piyush	
4.	SEQUENTIAL CIRCUIT	25/12/22	27/01/23			Piyush	

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ASSIGNMENT - 1

Que. 1 What is Number System?

Ans-1 When we type any letter or word, the computer translates then into numbers. Since computers can understand only numbers. A computer can understand only a few symbols called digits and these symbols describe different values depending on the position they hold in the numbers. In general, the binary number system is used in computers. However, the octal, decimal and hexa-decimal systems are also used sometimes.

Que. 2 What is Base?

Ans-2 A base is the available numbers in a numbering system. For example the most commonly known base is a base-10 numbering system or decimal numbers, which are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9. Another common base when dealing with computers is the binary base-2 which only has the numbers 0 and 1.

★ Types of Base -

1. Base - 2 (Binary)
2. Base - 8 (octal)
3. Base - 10 (Decimal)
4. Base - 16 (Hexa-decimal)
5. Base (BCD)
6. Base (Hamming)

Que. 3 Conversion of number Systems -

(i) Decimal to binary -

ex. 1 $(41)_{10} \rightarrow (101001)_2$

2	41	1
2	20	0
2	10	0
2	5	1
2	2	0
	1	

101001 Ans.

ex. 2 $(160)_{10} \rightarrow (10100000)_2$

2	160	0
2	80	0
2	40	0
2	20	0
2	10	0
2	5	1
2	2	0
	1	

(10100000) Ans.

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(ii) Binary to Decimal –

ex.1 $(1011)_2 \longrightarrow (11)_{10}$

$1\times2^3+0\times2^2+1\times2^1+1\times2^0$

$8+0+2+1$

11 Ans.

ex.2 $(1010\cdot011)_2 \longrightarrow (10\cdot375)_{10}$

$1\times2^3+0\times2^2+1\times2^1+0\times2^0 \cdot 0\times2^{-1}+1\times2^{-2}+1\times2^{-3}$

$8+0+2+0 \cdot 0+\frac{1}{4}+\frac{1}{8}$

$(10\cdot375)$ Ans.

(iii) Decimal to octal –

Ex.1 $(153)_{10} \longrightarrow (231)_8$

8	153	1
8	19	3
8	2	

(231) Ans.

Ex.2 $(127)_{10} \longrightarrow (177)_8$

8	127	7
8	15	7
8	1	

(177) Ans.

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(iv) Octal to decimal –

Ex.1 $(304)_8 \longrightarrow (196)_{10}$

$3 \times 8^2 + 0 \times 8^1 + 4 \times 8^0$

$= 3 \times 64 + 0 + 4$

$= 192 + 0 + 4$

$= (196)$ Ans.

Ex.2 $(1532)_8 \longrightarrow (858)_{10}$

$1 \times 8^3 + 5 \times 8^2 + 3 \times 8^1 + 2 \times 8^0$

$512 + 5 \times 64 + 24 + 2$

$512 + 320 + 26$

(858) Ans.

(v) Octal to Binary –

Ex.1 $(41)_8 \longrightarrow (100001)_2$

According to table $(100001)_2$ Ans.

Ex.2 $(77)_8 \longrightarrow (111111)_2$

According to table $(111111)_2$ Ans.

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(vi) Binary to Octal –

Ex.1 $(10011)_2 \longrightarrow (23)_8$

M-I → $(\ )_2 \longrightarrow (\ )_{10} \rightarrow (\ )_8$

$1\times2^4 + 0\times2^3 + 0\times2^2 + 1\times2^1 + 1\times2^0$

$16 + 0 + 0 + 2 + 1$

$(19)_{10}$

Now this decimal, Convert to octal

8	19	
8	2	3

$(23)_8$ Ans.

Ex.2 $(101100)_2 \longrightarrow (54)_8$

M-II → By Using table

I[st] making pair of three,

then putting the value from table

$(54)_8$ Ans.

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(vii) Hexa to Binary :-

Ex. 1 $(7A4)_{16} \rightarrow (11110100100)_2$

By Using table,

$(11110100100)_2$ Ans.

Ex. 2 $(5CA)_{16} \rightarrow (10111001010)_2$

By Using table,

$(10111001010)_2$ Ans.

(viii) Binary to Hexadecimal :-

Ex. 1 $(10101011)_2 \rightarrow (AB)_{16}$

By Using table, $(AB)_{16}$ Ans.

Ex. 2 $(100111011111)_2 \rightarrow (9DF)_{16}$

By Using table,

$(9DF)_{16}$ Ans.

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Que. If $(2x)_8 = (34)_x$

$$2\times8^1 + x\times8^0 = 3\times x^1 + 4\times x^0$$
$$16 + x = 3x + 4$$
$$16 - 4 = 3x - x$$
$$12 = 2x$$
$$\boxed{x = 6}$$ Ans.

Que. If $(121)_x = (125)_8$

$$1\times x^2 + 2\times x^1 + 1\times x^0 = 1\times8^2 + 2\times8^1 + 5\times8^0$$
$$x^2 + 2x + 1 = 64 + 16 + 5$$
$$x^2 + 2x + 1 = 85$$
$$x^2 + 2x - 84 = 0$$
$$\boxed{x = 8.2}$$

Que. If $(211)_x = (152)_8$

$$2\times x^2 + 1\times x^1 + 1\times x^0 = 1\times8^2 + 5\times8^1 + 2\times8^0$$
$$2x^2 + x + 1 = 64 + 40 + 2$$
$$2x^2 + x + 1 = 106$$
$$2x^2 + x - 105 = 0$$
$$\boxed{x = 7}$$ Ans.

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Que. Determine the base :

$$(23)_b + (44)_b + (14)_b + (32)_b = (223)_b$$

$$2\times b^1 + 3\times b^0 + 4\times b^1 + 4\times b^0 + 1\times b^1 + 4\times b^0 + 3\times b^1 + 2\times b^0 = 2\times b^2 + 2\times b^1 + 3\times b^0$$

$$2b+3+4b+4+b+4+3b+2 = 2b^2+2b+3$$

$$10b+13 = 2b^2+2b+3$$

$$0 = 2b^2+2b+3-13-10b$$

$$2b^2-8b-10=0$$

$$2b^2+2b-10b-10=0$$

$$2b(b+1)-10(b+1)=0$$

$$(2b-10)(b+1)=0$$

$\therefore b=5$, $b=-1$ (neglect)

$\boxed{b=5}$ **Ans.**

Que. $\sqrt{(41)_b} = (5)_b$ Find Base.

$$\sqrt{4\times b^1 + 1\times b^0} = 5\times b^0$$

$$\sqrt{4b+1} = 5$$

Squaring both side

$$4b+1 = 25$$

$$4b = 24$$

$\boxed{b=6}$ **Ans.**

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Que. 5 (i) Substraction with one's Complement :-

Ans-5)

1101011 − 111101

substract 1101011 from 111101

1st complement of (111101) is 000010

```
   1101011
 +  000010
   1101101
```

Ans => 0010010

(ii) Substraction with two's complement :-

1010101 − 1111000

(1111000) —2's→ 0000111

```
  0000111
 +      1
  0001000
```

```
  1010101
+ 0001000
  1011101  →  0100010
```

~~1011110~~

```
  0100010
 +      1
  0100011
```

0100011 Ans.

(iii) Substraction with Nine's complement :-

54321 − 12345

```
  99999       54321       41975
− 12345     + 87654     +     1
  87654     (1)41975      41976
```

41976 Ans.

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(iv) Substraction with Ten's Complements :-

215 − 155 = 1060

```
  999
 −155          215
  844         +845
 +  1         1060  Ans.
  845
```

Que. 6 Octal Addition :-

$(733)_8 + (421)_8 = (1354)_8$

According to Table

$(111011011)_2 + (100010001)_2$

```
   (1)  (1)(1)
    111011011
  + 100010001
  001011101100
```

$= (1354)_8$ Ans.

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★ Complement's -

① 1's complement →

Ex. - 100101
011010 Ans.

② 2's complement →

Ex. - (10010)

(10010) —1's→ 01101
+ 1
01110 Ans.

③ 9's complements -

Ex. - 786

999
- 786
213 Ans.

④ 10's complements →

Ex. 504 (504) —9's→ 999 − 504 = 495; 495 + 1 = 496 Ans.

★ x-3 Code / Excess-3 code :-

BCD
+ 0011 (Add 3)
x-3 code

Que. $(69)_{10} + (24)_{10} = (93)_{10}$

$(01101001)_{BCD} + (00100100)_{BCD}$

+ 0011 0011   0011 0011

$(10011100)_{x-3\ code}$ $(01010111)_{x-3\ code}$

```
  10011100
+ 01010111
  11110011
  MSB  LSB
```

```
   1111  0011
  -0011 +0011
  (1100  0110)BCD
-  0011  0011
   1001  0011
     9     3
```

$(93)_{10}$ Ans.

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★ **HEXA ADDICTION** –

$(C6F12)_{16} + (062C)_{16} = (~~6353E~~ \; C753E)_{16}$

According to the table

$(11000110111100010010)_2 + (00000110000101100)_2$

```
     ①①①
     11000110111100010010
+       0000001100 0101100
     11000111010100111110
```

$(C753E)_{16}$

★ **BCD Addition** –

Que. $(12)_{10} + (20)_{10} = (32)_{10}$

According to Table

$(00010010)_{\blacksquare} + (00100000)_{\blacksquare}$

```
  00010010
+ 00100000
  00110010  Ans.
```

↓

(32) Ans.

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★ BCD Substraction –

$(993)_{10} - (645)_{10} = (353)_{10}$

↓ 9's

$(998)_{10} + (354)_{10}$

```
  999
- 645
  354
```

```
  100110011000
+ 001101010100
  110011101100
+ 011001100110
 (1)001101010010
  |__________> +1
  001101010011  ——→  (353)10
```

Ans.

Que. A 7 bit hamming code is 1000111 if there is any error find location and correct it.

7	6	5	4	3	2	1
D_4	D_3	D_2	P_3	D_1	P_2	P_1
1	0	0	0	1	1	1

P-I 7531
1011
$x_1 = 1$

P-II 7632
1011
$x_2 = 1$

P-III 7654
1000
$x_3 = 1$

No. of one's = odd

x_3	x_2	x_1
1	1	1

▸ Error is on position 7.

x_3	x_2	x_1
1	1	1

Error on 7^{th} position there is our data (D_4).

ERROR ($1 \to 0, 0 \to 1$)

7	6	5	4	3	2	1
D_4	D_3	D_2	P_3	D_1	P_2	P_1
1	0	0	0	1	1	1

Correct → 0 0 0 0 1 1 1 Ans.

- Error occur at position 7. Here we see at position 7 we have the data (D_4) with value 1. So to correct the code we take "complement" of 1. So, the new 'Hamming Code' is **0000111**.

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Year 2022-23
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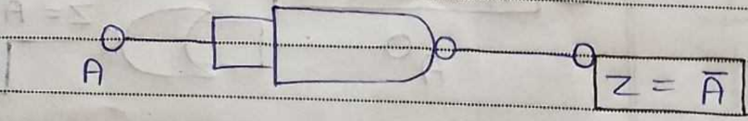
"ASSIGNMENT - 2"

"UNIT" - 2 LOGIC GATES

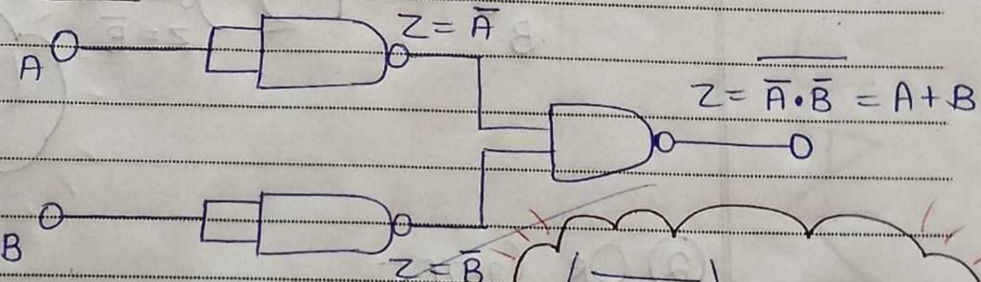
Que.1 Create "or", "not" & "and" gate with the help of 'Nand' gate ?

Ans-1 :-

① NOT GATE :-

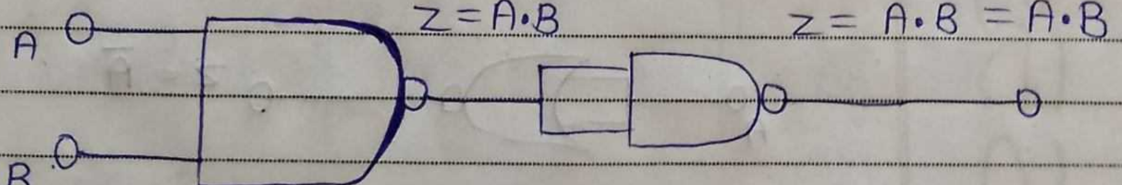


② OR GATE :-



$$\left(\overline{\overline{A} \cdot \overline{B}}\right) = A + B$$

③ AND GATE :-

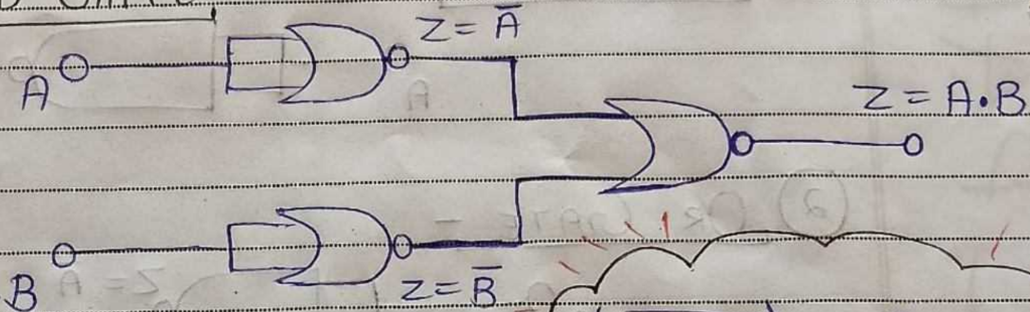


② C

Que. 2 Create "And", "or" & "Not" gate with the help of 'NOR'.

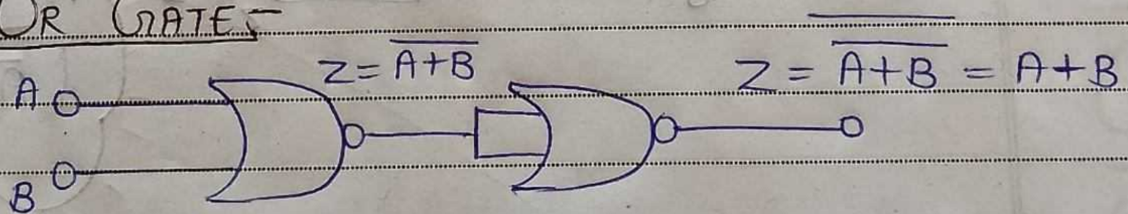
Ans-2 ⇒

① **AND GATE –**

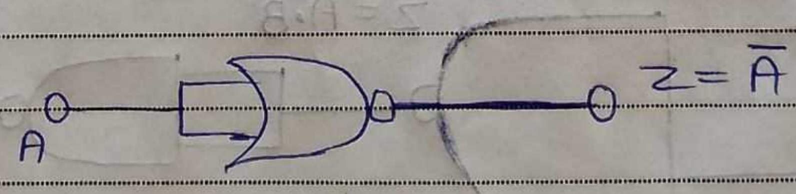


$$\left(\overline{\overline{A} + \overline{B}}\right) = A \cdot B$$

② **OR GATE –**



③ **NOT GATE –**



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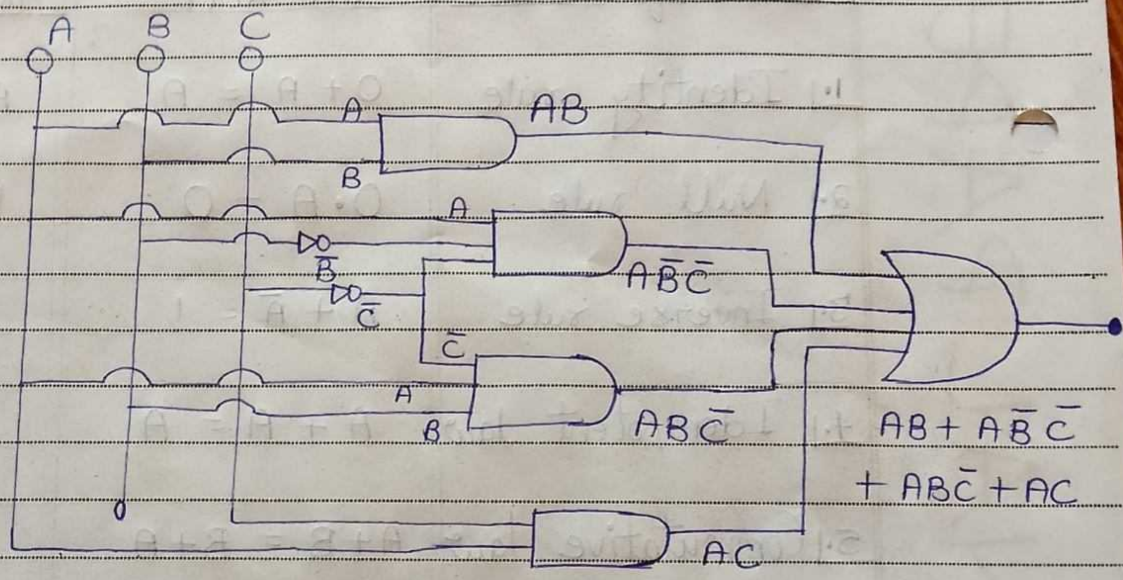
Que. 3 Write the Boolean Algebra rules?

Ans-3 =>

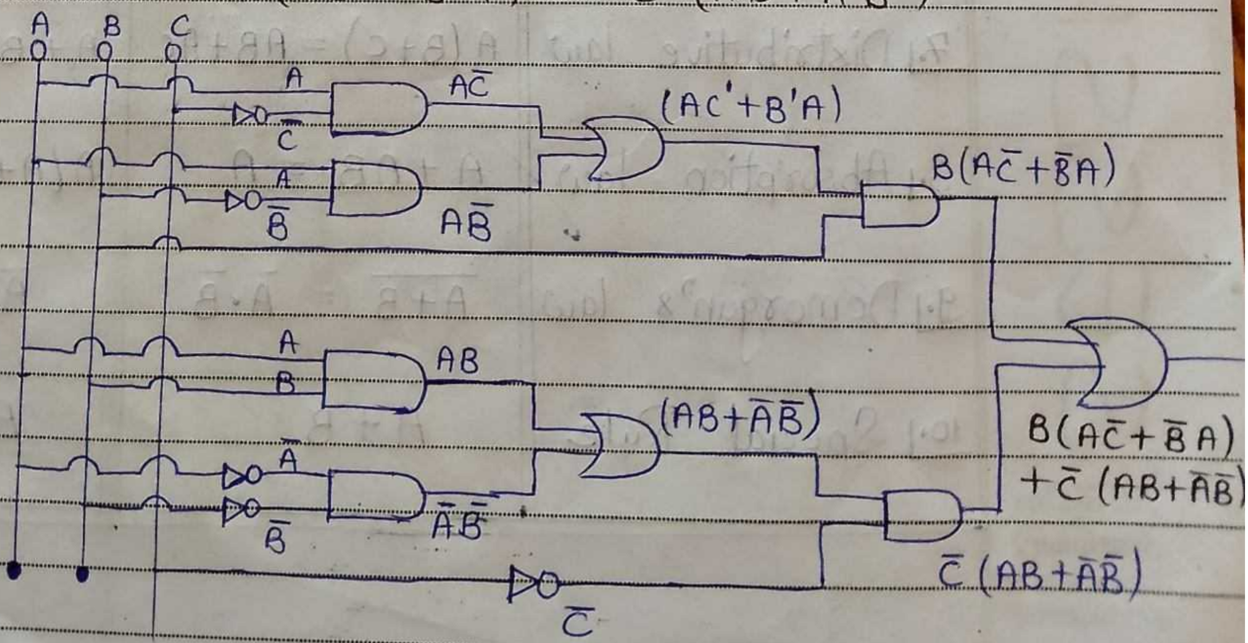
BOOLEAN ALGEBRA

Name of Rule	OR RULE	AND RULE
1. Identity rule	$0 + A = A$	$A \cdot 1 = A$
2. Null rule	$0 \cdot A = 0$	$1 + A = 1$
3. Inverse rule	$A + \bar{A} = 1$	$A \cdot \bar{A} = 0$
4. Idempotent law	$A + A = A$	$A \cdot A = A$
5. Commutative law	$A + B = B + A$	$AB = BA$
6. Associative law	$(A+B)+C = A+(B+C)$	$(AB)C = A(BC)$
7. Distributive law	$A(B+C) = AB + AC$	$A + BC = (A+B) \cdot (A+C)$
8. Absorption law	$A + AB = A$	$A(A+B) = A$
9. Demorgan's law	$\overline{A+B} = \bar{A} \cdot \bar{B}$	$\overline{AB} = \bar{A} + \bar{B}$
10. Special Rule	$A + B$	$A + \bar{A}B$

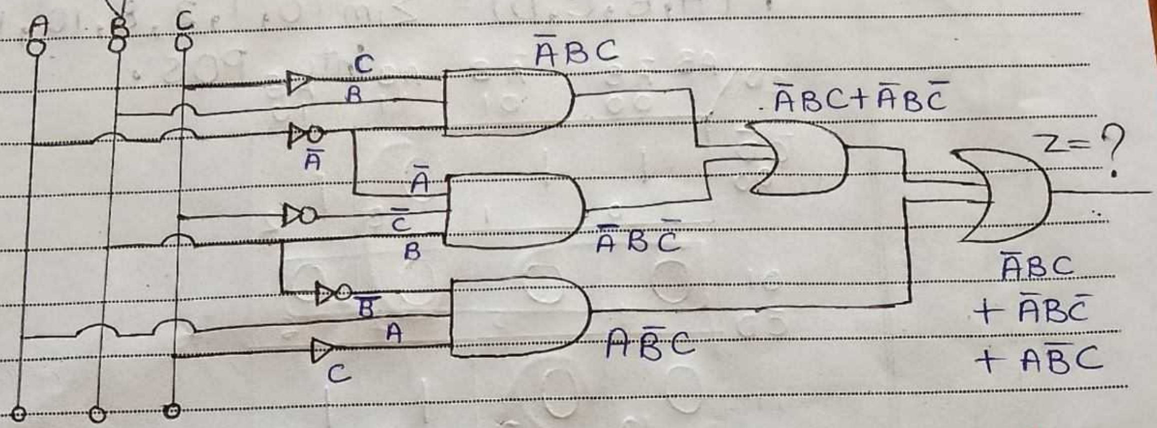
Que. 4 Draw logic gate diagram of the eq.^{n} – $AB + A\bar{B}\bar{C} + AC + AB\bar{C}$



Que. 5 Draw logic gate diagram of the eq.^{n} – $B(AC' + B'A) + C'(AB + A'B')$



Que. 6. Write the equation of the following logic gate ?



Final Ans => $Z = \text{"}\bar{A}BC + \bar{A}B\bar{C} + A\bar{B}C\text{"}$

Que. 7 Find SOP of $F(A,B,C,D) = \Sigma m(0,1,2,5,7,8,9,10,13,15)$.

CD \ AB	$\bar{A}\bar{B}$ 00	$\bar{A}B$ 01	AB 11	$A\bar{B}$ 10
$\bar{C}\bar{D}$ 00	1 (0)	1 (1)	(3)	1 (2)
$\bar{C}D$ 01	(4)	1 (5)	1 (7)	(6)
CD 11	(12)	1 (13)	1 (15)	(14)
$C\bar{D}$ 10	1 (8)	1 (9)	(11)	1 (10)

Final Ans. => $\bar{B}\bar{D} + \bar{A}\bar{D} + BD$ Ans.

Que. 8 Convert SOP into POS of the function

$F(A,B,C,D) = \sum m(0,1,2,8,10,11,14,15)$ into POS.

CD \ AB	$\bar{A}\bar{B}$ 00	$\bar{A}B$ 01	AB 11	$A\bar{B}$ 10
$\bar{C}\bar{D}$ 00	1 [0]	1 [1]	0 [3]	1 [2]
01 $\bar{C}D$	0 [4]	0 [5]	0 [7]	0 [6]
11 CD	0 [12]	0 [13]	1 [14]	1 [15]
10 $C\bar{D}$	1 [8]	0 [9]	1 [11]	1 [10]

$\Rightarrow \bar{C}D + \bar{A}D + AB\bar{C} + \bar{A}BC$

Final Ans.

$(\bar{C}+D)(\bar{A}+D)(A+B+\bar{C})(\bar{A}+B+C)$

Take whole bar

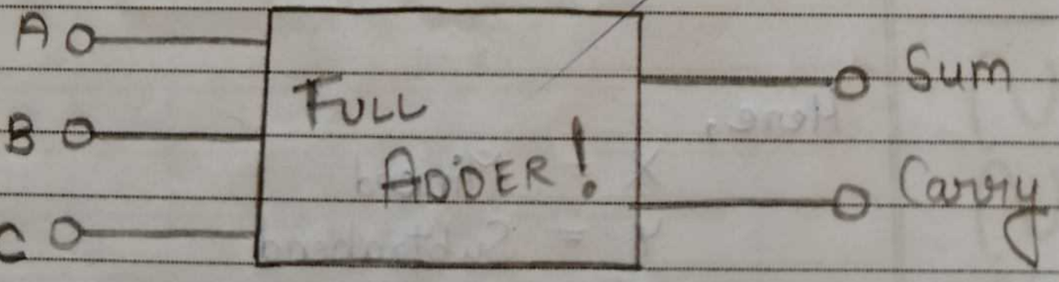
Ans. $(C+\bar{D})(A+\bar{D})(\bar{A}+B+C)(A+\bar{B}+\bar{C})$

"ASSIGNMENT - 3"

Que. 1 Short Note on Full Adder.

Ans-1) A full adder is a digital circuit that performs addition. It adds three inputs & produces two outputs. The first two inputs are A & B and the third input is an input carry as C in. The output carry is designed as Cout and the normal output is designated as S which is Sum.

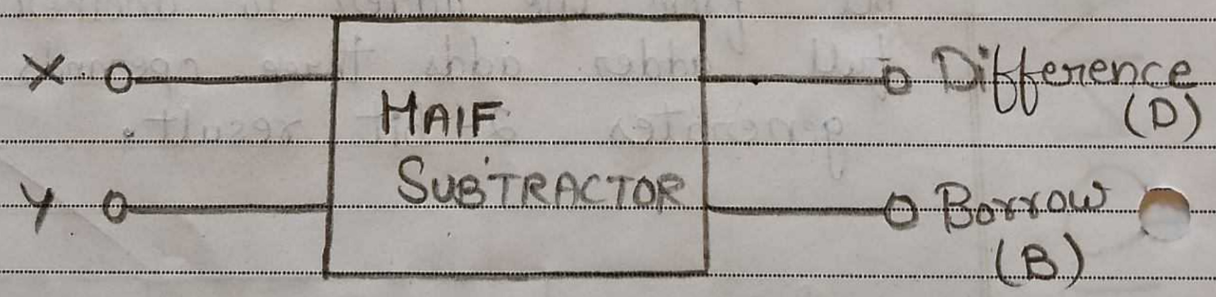
A full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to another. A 1-bit full adder adds three operands and generates 2-bit result.



"FULL ADDER"

Que. 2 Short note on Half - Subtractor ?

Ans-2) Half - Subtractor is a combinational circuit with two - inputs (let say x & y) and two outputs which are 'differente' and 'borrow'. It produces the difference between two binary bits at the input and also produces an output (Borrow) to indicate if a 1 has been borrowed. In the subtraction (X - Y), X is called a Minuend bit and Y is called as Subtrahend bit.



Here,

X = Minuend

Y = Subtrahend

B = Borrow

D = Difference

"HALF SUBTRACTOR"

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Que. 3 Implement a mux for boolean function.

$F(A, B, C) = \Sigma(1, 3, 5, 6)$ if (C) is a input.

Sol.^{n} ⇒ $F(A, B, C) = \Sigma(1, 3, 5, 6)$

A, B → Select line; C → Input

Select line $n = 2$

$2^n \times 1$

$2^2 \times 1$

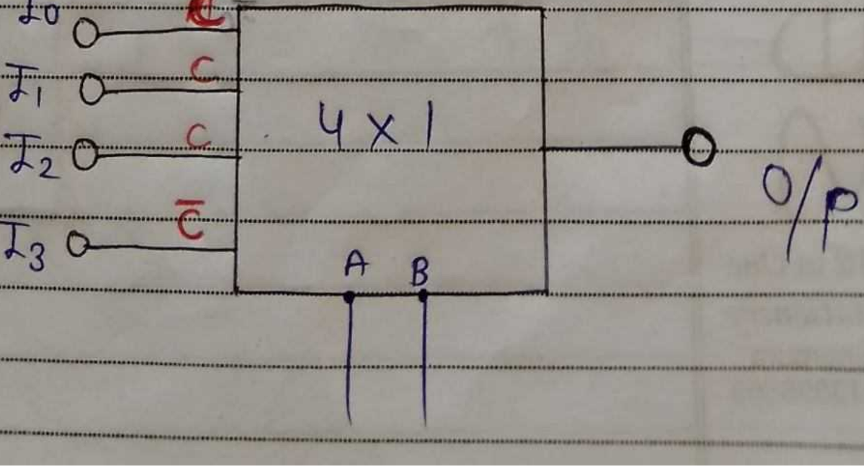
4×1

4 → Input, 1 → Output

	A	B	C
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

	I_0	I_1	I_2	I_3
$\bar{C}$	0	2	4	6
C	1	3	5	7
	C	C	C	$\bar{C}$

$\bar{C} = 0$
$C = 1$

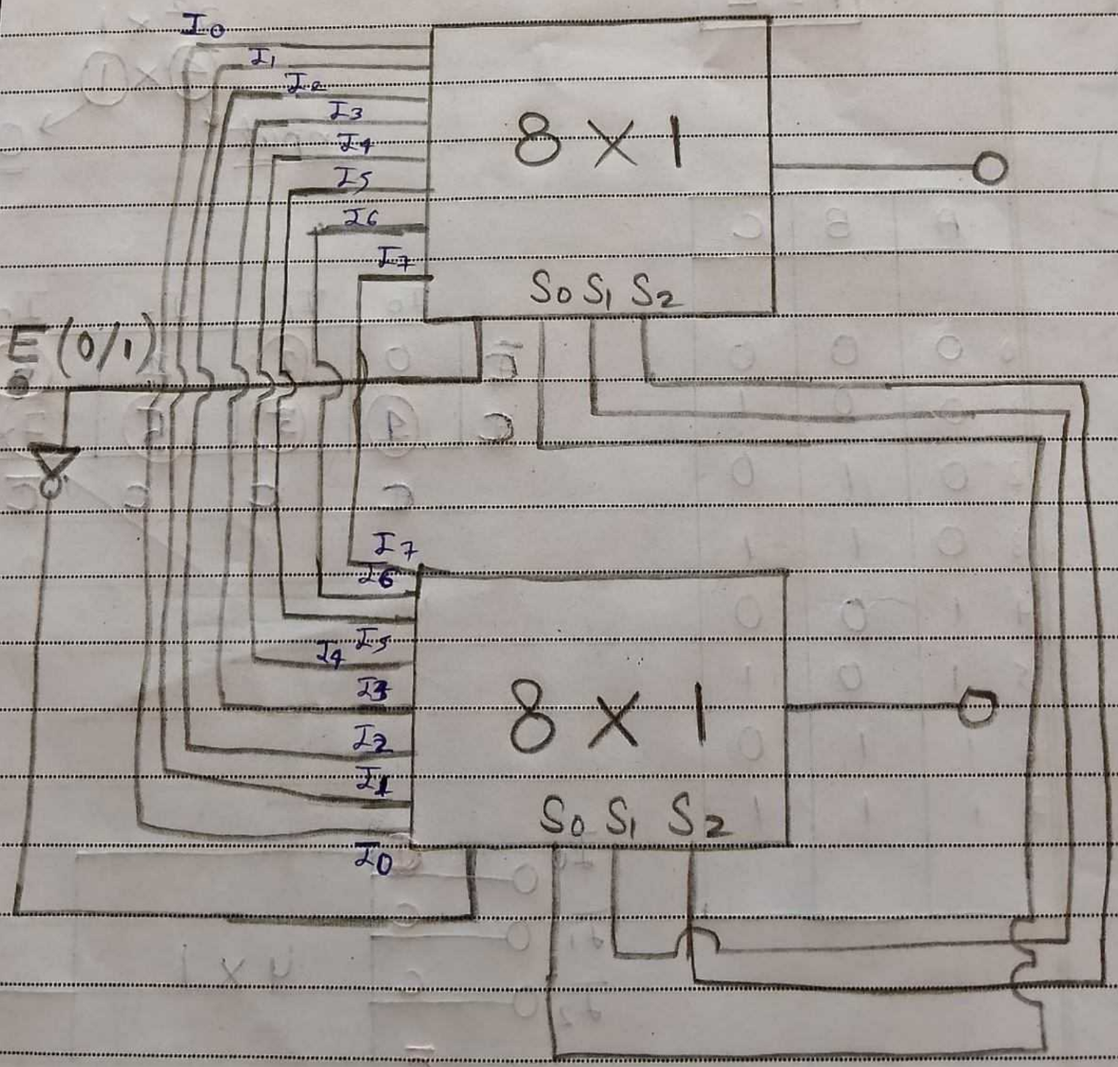


Que. 4 Obtain 16×1 Mux with 8×1 Mux.

Sol. ⇒ Here, S_1 & S_2 → Select lines

8 inputs → $I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7$

E = Enable switch (0/1)



Year ....

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Que. 5. It is necessary to sum two binary no. each two bit long in order to form then addition in binary. Let the two no. be represented by a_1a_0 and b_1b_0 where significiant bit. Determine the no. of output line required and find the simplifie boolean algebra.

Input		Output			
$a_1 a_0$	+ $b_1 b_0$	P	Q	R	S
0 0	0 0	0	0	0	0
0 0	0 1	0	0	0	1
0 0	1 0	0	0	1	0
0 0	1 1	0	0	1	1
0 1	0 0	0	0	0	1
0 1	0 1	0	0	1	0
0 1	1 0	0	0	1	1
0 1	1 1	0	1	0	0
1 0	0 0	0	0	1	0
1 0	0 1	0	0	1	1
1 0	1 0	0	1	0	0
1 0	1 1	0	1	0	1
1 1	0 0	0	0	1	1
1 1	0 1	0	1	0	0
1 1	1 0	0	1	0	1
1 1	1 1	0	1	1	0

P = 0

★ **K-Maps :-**

Q

a_1a_0 \ b_1b_0	$\bar b_1 \bar b_0$	$\bar b_1 b_0$	$b_1 b_0$	$b_1 \bar b_0$
$\bar a_1 \bar a_0$	0	1	3	2
$\bar a_1 a_0$	4	5	1 (7)	6
$a_1 a_0$	12	1 (13)	1 (15)	1 (14)
$a_1 \bar a_0$	8	9	1 (11)	1 (10)

$a_0 b_1 b_0 + a_1 a_0 b_0 + a_1 b_1$ ⇐

R

a_1a_0 \ b_1b_0	$\bar b_1 \bar b_0$	$\bar b_1 b_0$	$b_1 b_0$	$b_1 \bar b_0$
$\bar a_1 \bar a_0$			1	1
$\bar a_1 a_0$		1		1
$a_1 a_0$	1		1	
$a_1 \bar a_0$	1	1		

$\Rightarrow \bar a_1 \bar a_0 b_1 + \bar a_1 b_1 \bar b_0 + \bar a_1 a_0 \bar b_1 b_0 + a_1 a_0 b_1 b_0 + a_1 \bar b_1 \bar b_0 + a_1 \bar a_0 \bar b_1$

S

a_1a_0 \ b_1b_0	$\bar b_1 \bar b_0$	$\bar b_1 b_0$	$b_1 b_0$	$b_1 \bar b_0$
$\bar a_1 \bar a_0$		1	1	
$\bar a_1 a_0$	1			1
$a_1 a_0$	1			1
$a_1 \bar a_0$		1	1	

$a_0 \bar b_0 + \bar a_0 b_0$ ⇐

★ **No. of Output line = 3 Ans.**

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ASSIGNMENT-4

UNIT-4 SEQUENTICIAL CIRCUIT

Que.1 Write the difference between Combinational circuit and sequenticial circuit.

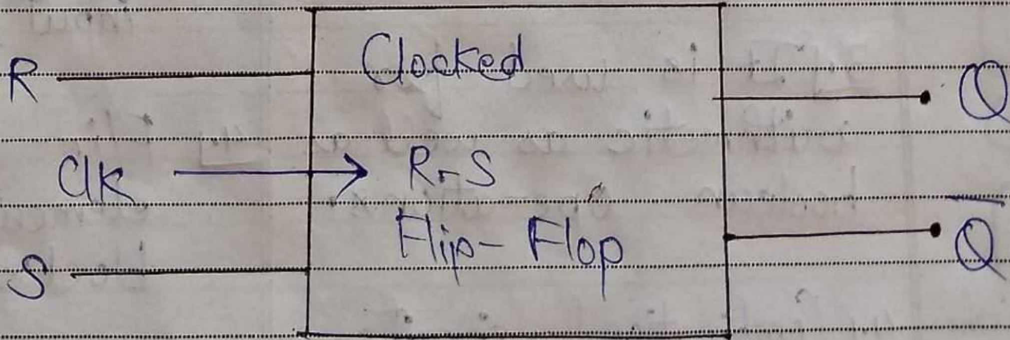
Ans-1

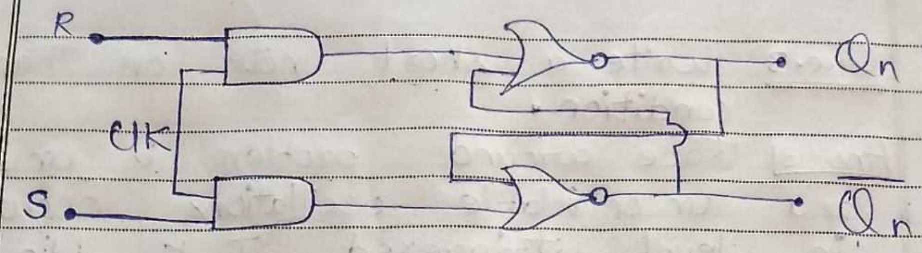
Combinational Circuit	Sequenticial Circuit
1.) It contains logic gates but do not contain storage element on memory element.	1.) It contains logic gates as well as memory element.
2.) Logic gates are connected together to give a specific output for certain input variables.	2.) It is mainly used for storing data.
3.) It is used for arithmetic as well as boolean operations.	3.) In this output depends upon present as well as past input.
4.) Combinational circuits don't have clock, they don't require triggering.	4.) Flip-flops are elementary building blocks.

5.1 These types of circuits are defined as the time indepedent circuit which do not depends upon previouts inputs to generate any outputs.	5.1 Sequential Circuits are those which are dependent on clock cycle hence they - requir triggering & also this is time dependent.

Que.2 Describe Clocked R.S flip-flop.

Ans-2) In addition to the R(reset) & S(set) inputs, these circuits also receive the clock signals. In the clocked R-S flip-flop the Q output will be unaffected by any change in R (or) S as long as the clock (C) is 0 (Low). That is during the "read" phase of the clock cycle the contents of memory connect be changed.





★ Characteristic Table :-

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

★ Truth Table :-

S	R	CLK	Q_n
X	X	0	Q_n
0	0	1	Hold
0	1	1	0
1	0	1	1
1	1	1	Invalid

★ Excitation Table :-

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

★ K-Map :-

Q_{n+1}

	$\overline{R}\,\overline{Q}_n$	$\overline{R}Q_n$	RQ_n	$R\overline{Q}_n$
$\overline{S}$		1		
S	1	1	X	X

$$Q_{n+1} = S + \overline{R}Q_n$$

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Que.3 Write a short note on Race-around condition.

Ans-3) Race around problem is unwanted and uncontrolable oscillations occuring in level triggered J K flip-flop due to a feedback from output to input. It is overcome by master-slave configuration.

Race around condition in JK flip-flop are as follows:

- For J.K flip-flop, if J=K=1, if clk = 1 for a long period of time, then output (Q) will toggle as long as clk remains high which makes the outputs unstable or uncertain.

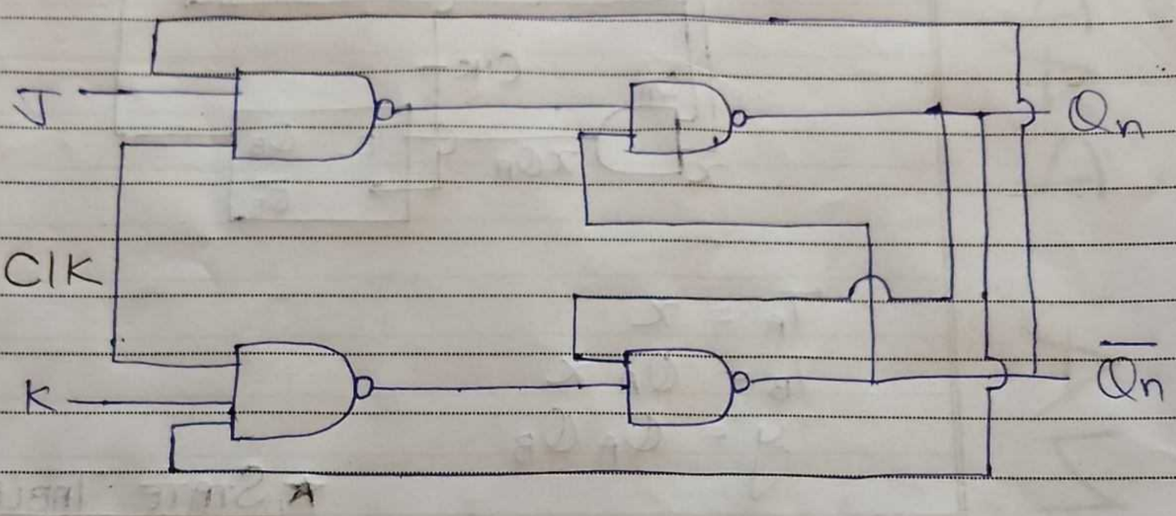
This is called a race around condition in J.K flip-flop.

★ Conditions -

1. Level Triggered
2. J=K=1, Q ⇒ Toggle
3. $T_w >> T_d$ (where T_d = Time taken by the flip-flop to proceed the input)

• **NOTE** –

When all the above 3 conditions fulfill or occur then only race around conditions occurs in J.K flip-flops.

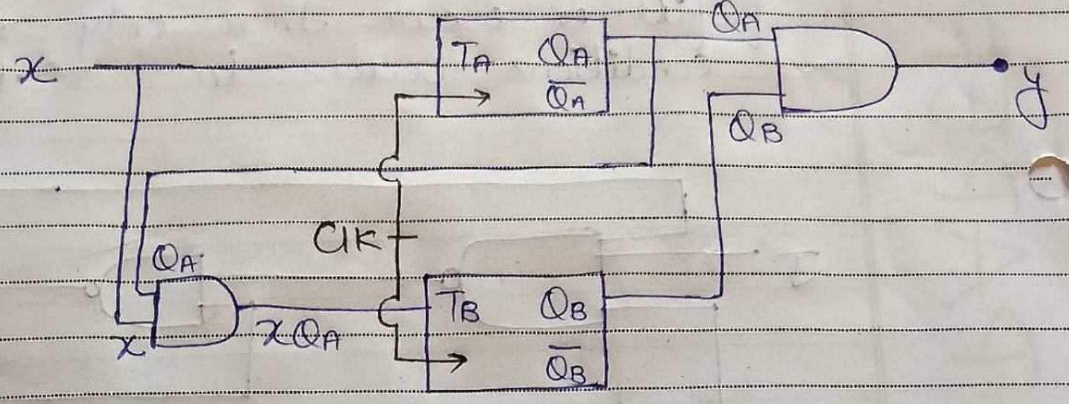


0 1 0 1

1 0 1 0

} Toggle

Que. 4 Analysis of sequential circuit with T flip-flop.



$T_A = x$

$T_B = Q_A x$

$y = Q_A Q_B$

★ STATE TABLE :-

Previous State		Input	Next State				Output
Q_A	Q_B	x	Q_A^+	Q_B^+	T_A	T_B	y
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0
0	1	0	0	1	0	0	0
0	1	1	1	1	1	0	0
1	0	0	1	0	0	0	0
1	0	1	0	1	1	1	0
1	1	0	1	1	0	0	1
1	1	1	0	0	1	1	1

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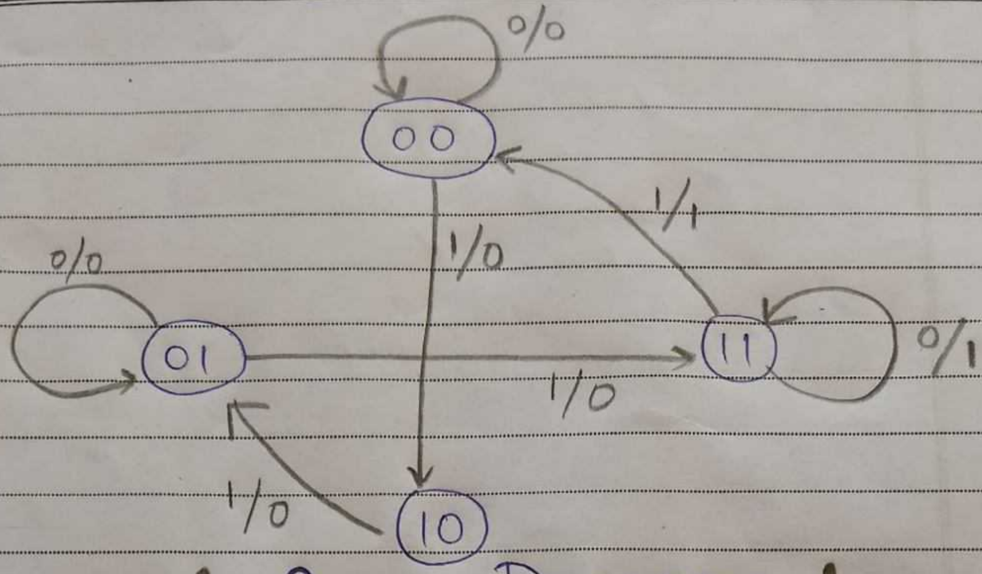

— : STATE DIAGRAM : —

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